What is claimed is:

1. A semiconductor device comprising:

an SOI substrate having a semiconductor substrate, a dielectric layer, and a semiconductor layer formed in this order;

a transistor having a drain region and a source region respectively formed in said semiconductor layer, and a gate electrode formed via a gate dielectric film on a channel region sandwiched between said drain region and said source region;

an interlayer dielectric film formed on said transistor;

a drain wiring and a source wiring formed on said interlayer dielectric film;

a first conductor formed in said interlayer dielectric film for connecting said drain wiring to said drain region; and

a second conductor formed in said interlayer dielectric film for connecting said source wiring to said source region, wherein

said drain region has a first part being adjacent to said channel region and a second part formed to protrude from said first part so that a part of outer peripheries of said drain region extends away from said gate electrode in a plan view, and

said first conductor is connected to said second part of said drain region.

2. The semiconductor device according to claim 1, wherein said first part of said drain region has a width of 0.2 to 0.5 μm with respect to a channel length direction of said channel region, and said second part of said drain region has a length of 0.1 to 0.5 μm with respect to a direction protruding from said first part of said drain region.

3. The semiconductor device according to claim 1, wherein

said first part of said drain region has a plurality of corner parts in a plan view, and

said second part of said drain region is formed to protrude obliquely with respect to a channel width direction of said channel region from said corner part which is not adjacent to said gate electrode.

4. The semiconductor device according to claim 1, wherein a bottom surface of said first conductor is partially in contact with said second part of said drain region by being shifted away from said gate electrode.

5. The semiconductor device according to claim 1, wherein said source region has a first part being adjacent to said channel region and a second part formed to protrude from said first part so that a part of outer peripheries of said source region extends away from said gate electrode in a plan view, and

said second conductor is connected to said second part of said source region.

6. The semiconductor device according to claim 5, wherein said first part of said source region has a width of 0.2 to 0.5 μm with respect to a channel length direction of said channel region, and said second part of said source region has a length of 0.1 to 0.5 μm with respect to a direction protruding from said first part of said source region.

7. The semiconductor device according to claim 5, wherein

said first part of said source region has a plurality of corner parts in a plan view, and

said second part of said source region is formed to protrude obliquely with respect to a channel width direction of said channel region from said corner part which is not adjacent to said gate electrode.

8. The semiconductor device according to claim 5, wherein a bottom surface of said second conductor is partially in contact with said second part of said source region by being shifted away from said gate electrode.

9. The semiconductor device according to claim 1, wherein said source region has a first part being adjacent to said channel region, and

said second conductor is connected to said first part of said source region.

10. The semiconductor device according to claim 1, wherein

said transistor further has a side wall formed on a side surface of said gate electrode, and

said side wall is constructed with a porous material.

11. The semiconductor device according to claim 1, wherein said interlayer dielectric film is formed except for a region between said gate electrode and said first and second conductors.

12. A semiconductor device comprising:

a substrate;

a transistor having a pair of source/drain regions formed in said substrate, a gate electrode formed via a gate dielectric film on a channel region sandwiched between said pair of source/drain regions, and a side wall formed on a side surface of said gate electrode;

an interlayer dielectric film formed on said transistor;

source/drain wirings formed on said interlayer dielectric film; and

conductors formed in said interlayer dielectric film for connecting said source/drain wirings to said source/drain regions, wherein

said side wall is constructed with a porous material.

13. A semiconductor device comprising:

a substrate;

a transistor having a pair of source/drain regions formed in said substrate, and a gate electrode formed via a gate dielectric film on a channel region sandwiched between said pair of source/drain regions;

an interlayer dielectric film formed on said transistor;

source/drain wirings formed on said interlayer dielectric film; and

conductors formed in said interlayer dielectric film for connecting said source/drain wirings to said source/drain regions, wherein

said interlayer dielectric film is formed except for a region between said gate electrode and said conductors.